Put the Pieces Together in the Materials Space: Advanced Materials Solutions for 10nm and Beyond

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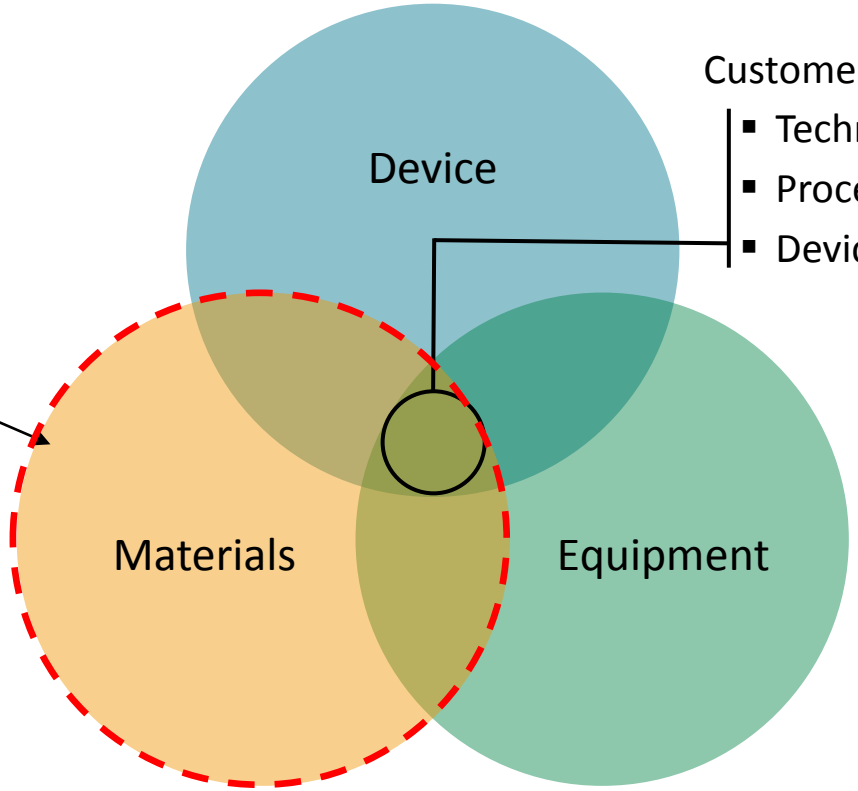
Entegris

creating a material advantage

Increasing Interdependency Within the Semiconductor Ecosystem to Meet Performance, Yield and Cost Targets for 10nm and Beyond

Opportunity to "put the pieces together" in the materials space

- Advanced precursors, advanced surface preparation, novel doping
- Materials, handling, sensing, and delivery components
- Enabling new paradigms



Significant overlap within the Semiconductor Ecosystem

- Increasing need to work together in this space for advanced solution
- Targeted collaborations are key to the challenges advanced node

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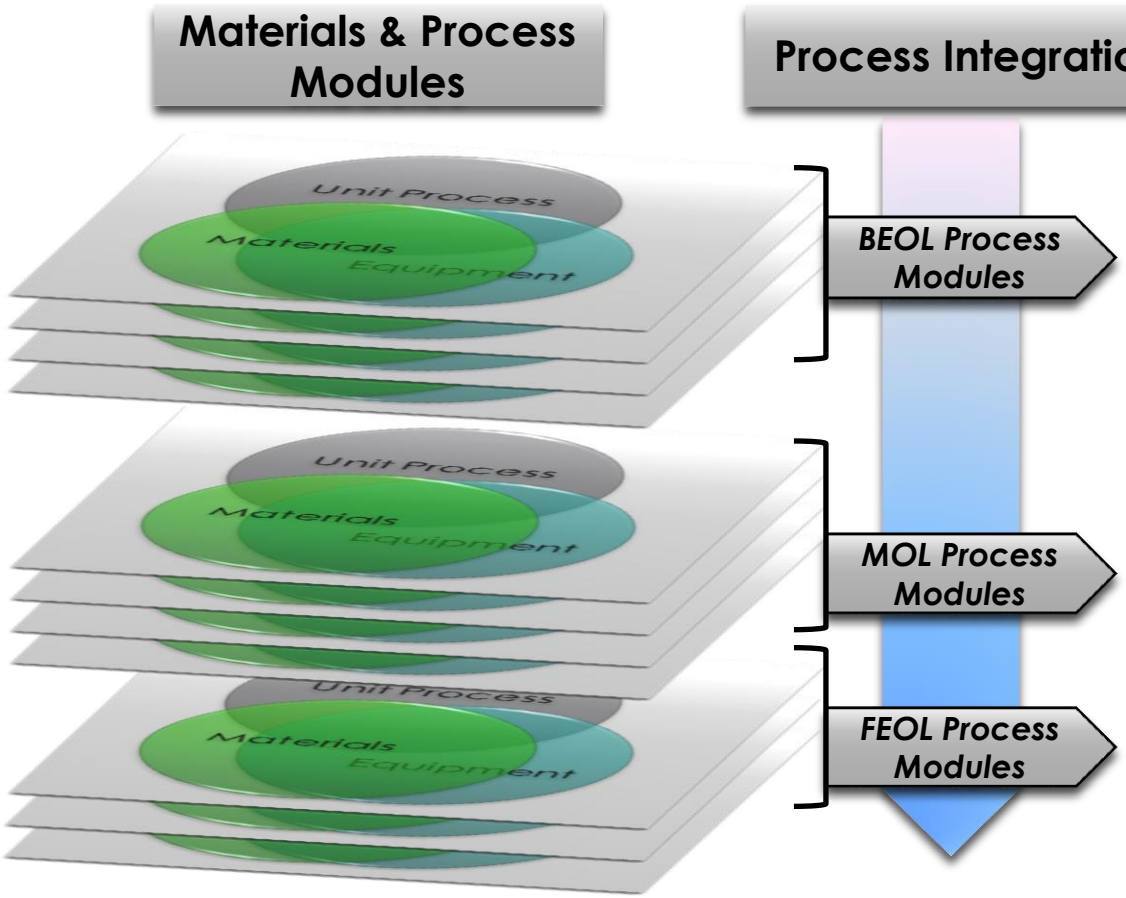
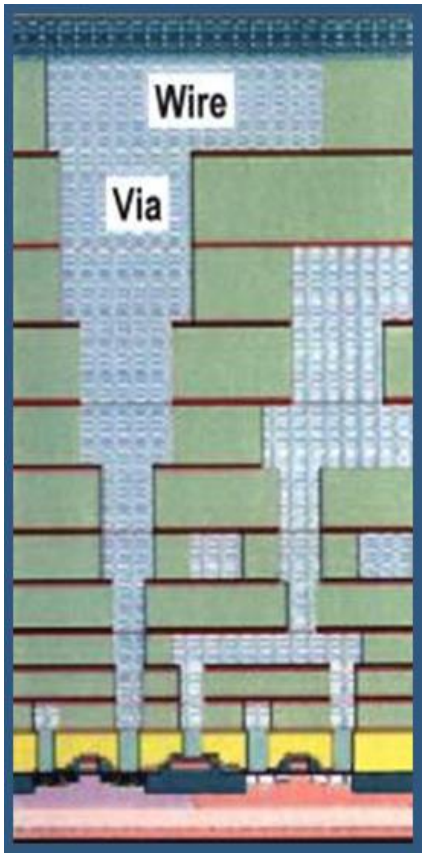
Increased Interaction Among Wet, Deposition, Implant, and Plating Processes When Integrating Materials





Understanding the integrated stack and material interactions enables tailored solutions that fit customer requirements

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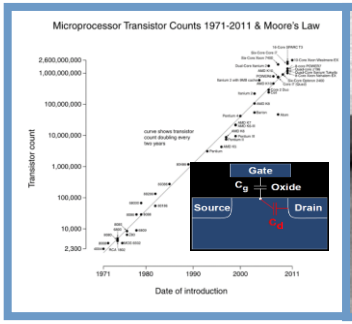
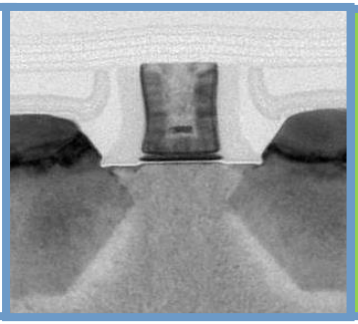
FEOL: New Channel Materials and 3D Structures

90nm → 45nm → 16nm → 7nm/5nm

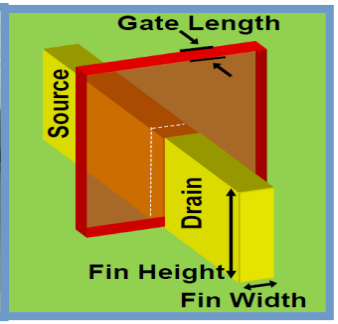
Dimensional scaling → **New Materials** → **New Structures**



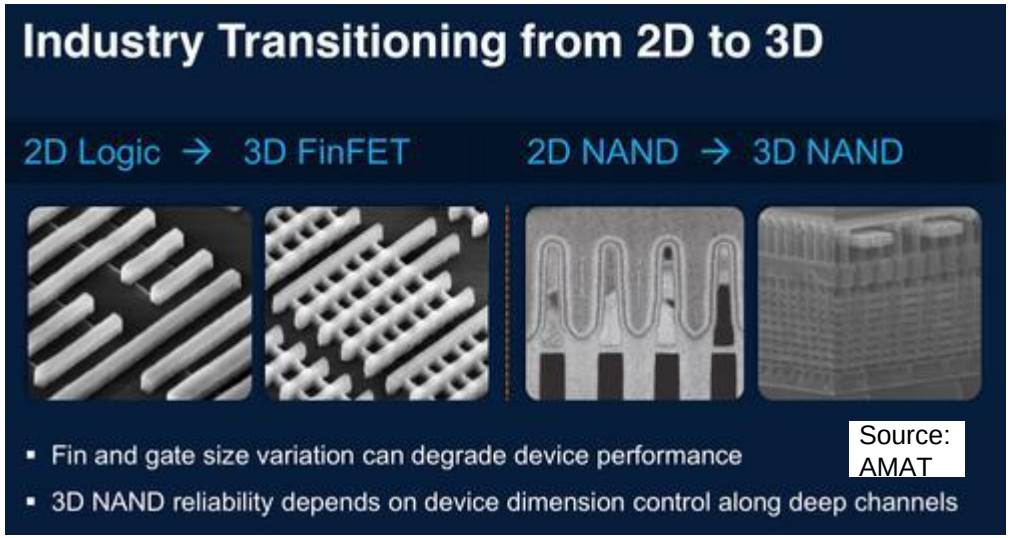
Dimensional scaling was the main driving force of in the past 50 years



High-K/Metal gate transistor improved performance, Intel

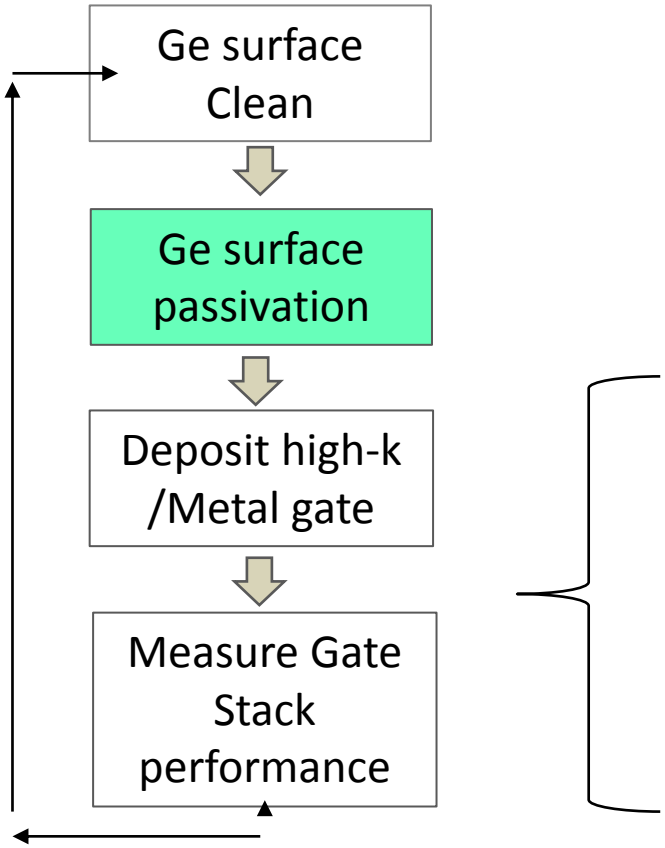


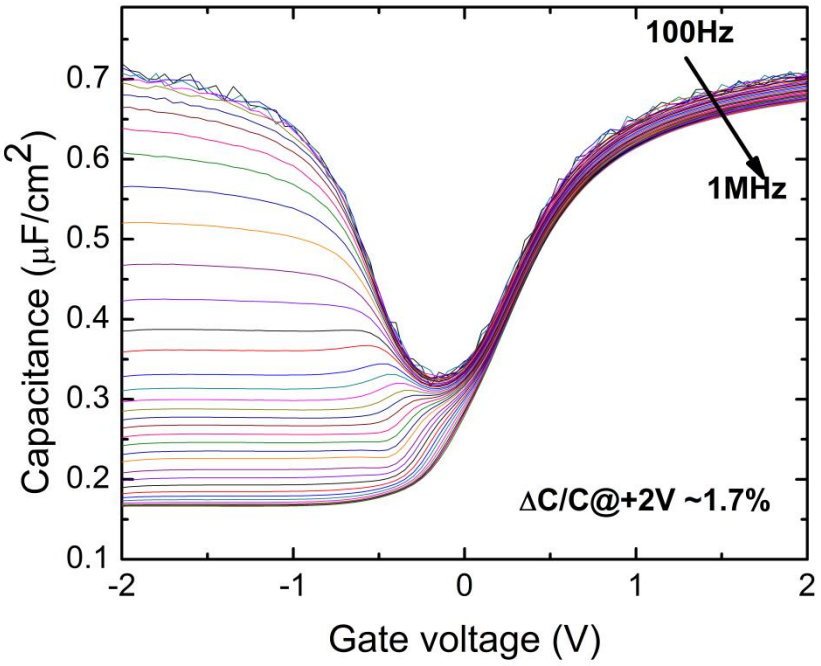
FinFET and Trigate is structure renovation



- **New Channel Materials**
  - **e.g. SiGe, III-V, …**
  - **Need: Surface passivation clean**
- **New high-k materials and deposition**
  - **Need: High-K and metal gate tailoring to best performance**
- **New device structure**
  - **e.g. SiGe Nano wire**
  - **Need: Ge/SiGe selective etch**
- **Ultra shallow junction with high surface conformal doping in 3D device structure**
  - **Need: New Doping Scheme**

Entegris Uses Electrical Testing To Evaluate Ge Surface Passivation and Queue Time Improvement





Frequency dispersion at accumulation region is 1.7%

Results from Entegris/NCTU Collaboration on Ge Surface Passivation

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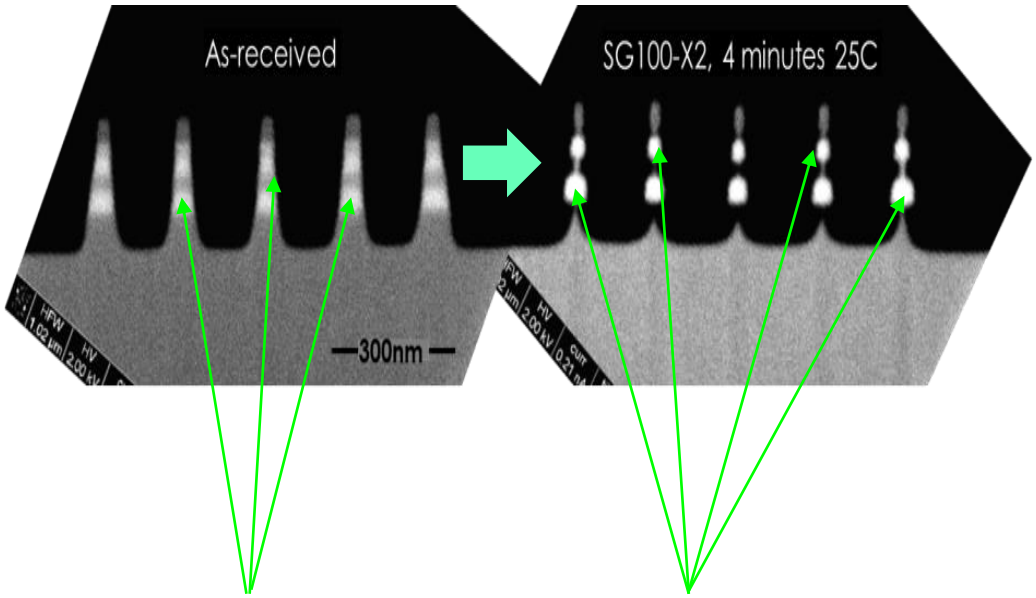
Stack of Ge Nanowires Formed By Selective SiGe Etching for Ge Mano Wire-Based Gate-All-Around FETs

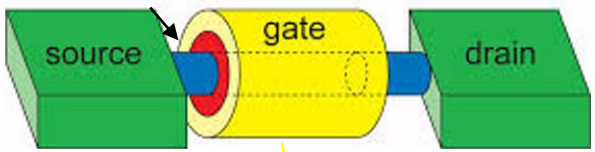
Before Selective Etch ***after Selective Etch***

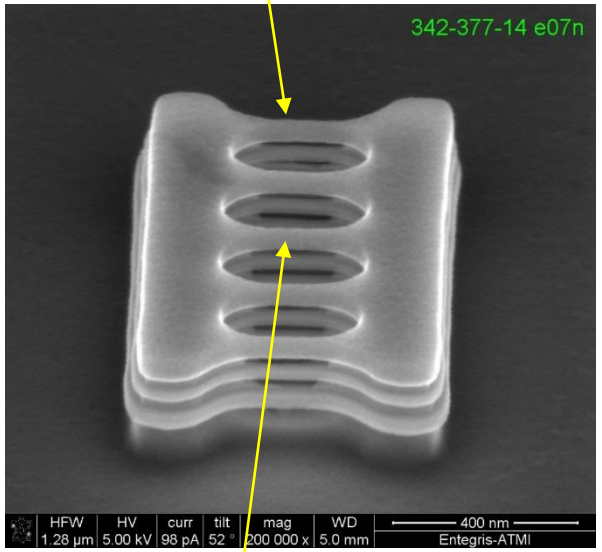


SiGe/Ge/SiGe/G stack in Fins

Cross-Sectional View of Ge Nano wires After etch removal of SiGe

Ge nano wire





3D SEM View of Ge Nano wires after selective etch removal of SiGe

SiGe: Ge etch > 20:1

Results from Entegris-IMEC JDP on FEOL cleans/etches

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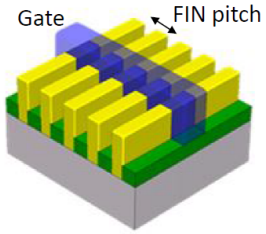
As MLD (Monolayer Doping) on Si and Ge Achieved ~Monolayer Coverage Of Doping On Ge Surface

1. Pitch Scaling for Logic Devices

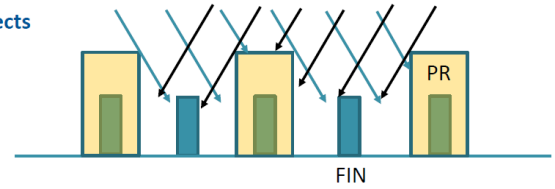


Node	14nm	10nm	7nm	5nm
FIN width	7.6	7.2	6.8	6.4
FIN pitch	60	48	38	30
L_G (nm)	20	14	11.7	9.7
Gate Pitch	80	64	50	40

ITRS 2013

N5nm: FIN pitch will be ≤ 30 nm→ increasingly difficult to achieve conformal doping with tilted implant

2. Shadowing Effects



Monolayer Doping Process

- Conformal, damage-free, shallow junction, cost-effective

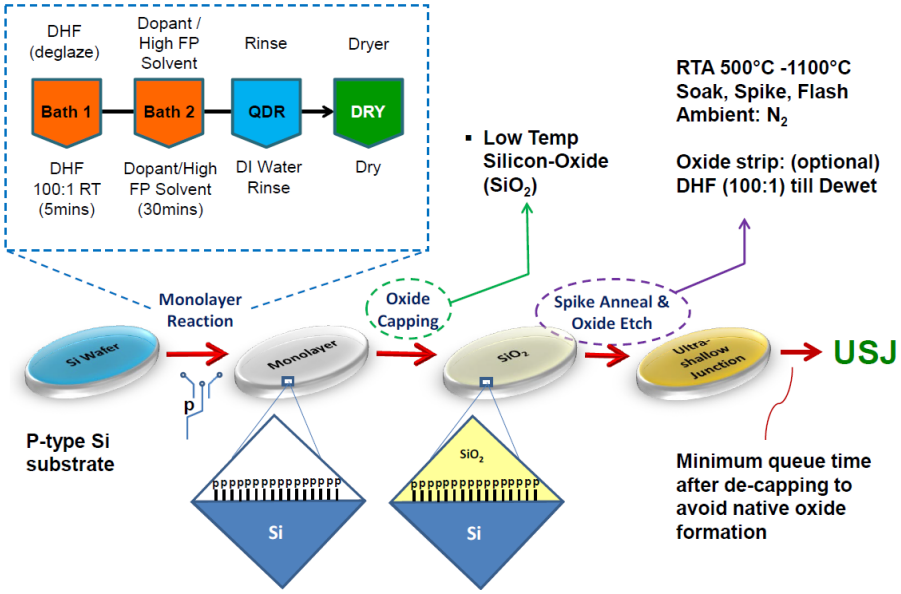
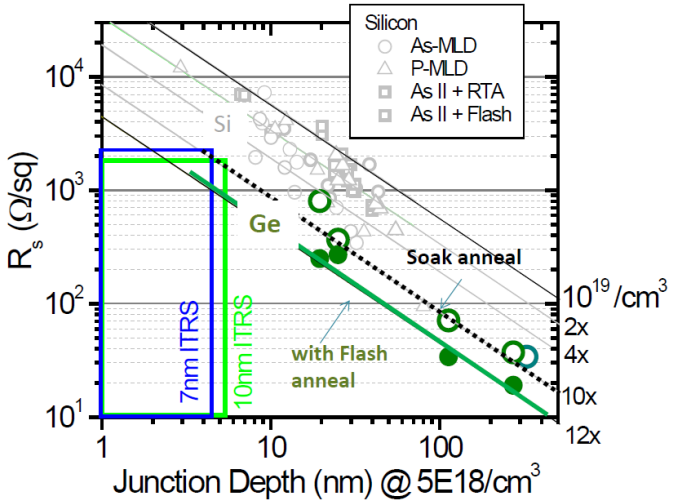


Figure of Merit for As-MLD in Si and Ge

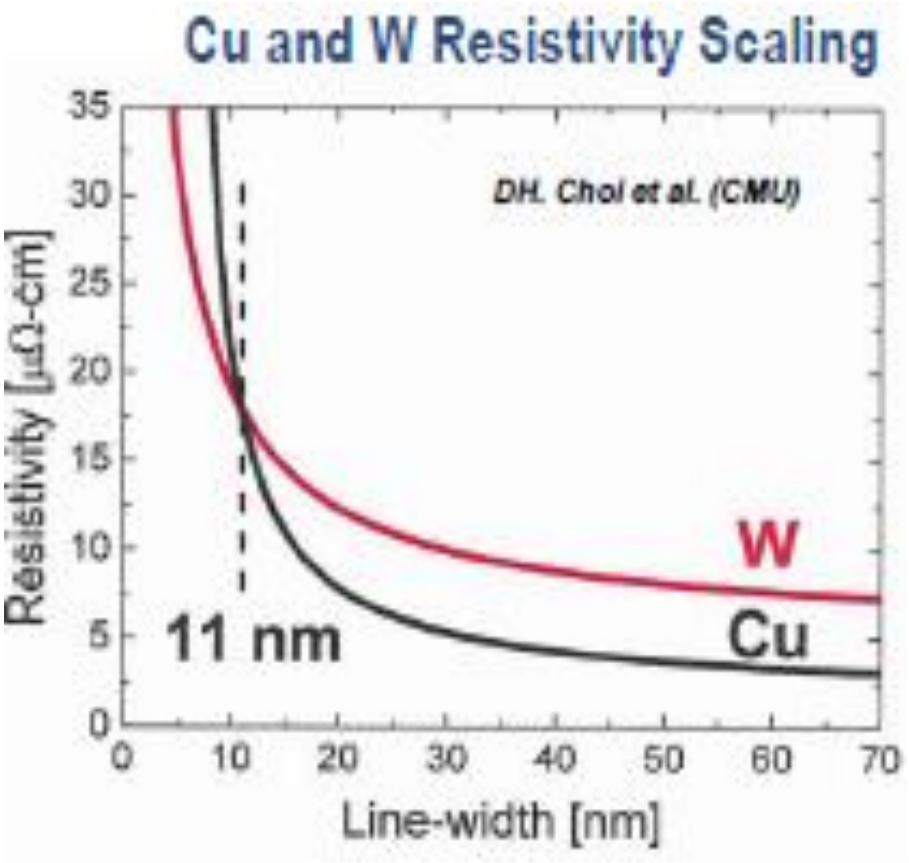


Ref: Lee *et al*, SEMATECH Surface Preparation and Cleaning Conference (SPCC), 2015

Results from Entegris-SEMATECh JDA

Entegris

BEOL/MOL Challenges: Performance, Yield, and Cost



Thin film sheet resistance trend W vs. Cu

Device Scaling causing interconnect challenges

- Line resistivity increasing due to Cu electron free mean path and film roughness makes Cu unfavorable as its resistivity will shoot up.
- Reliability issues due to Cu electro-migration below 20 nm
- High aspect ratio features causing yield issues (e.g. voids in plating solution)

Alternative interconnect metals

- Al, Co and W are alternatives
  - display better sheet resistance vs. Cu at <20nm
- Al displays poor EM performance
- Co displays better EM performance
  - can be deposited by ALD, CVD, plating
  - can be integrated into device

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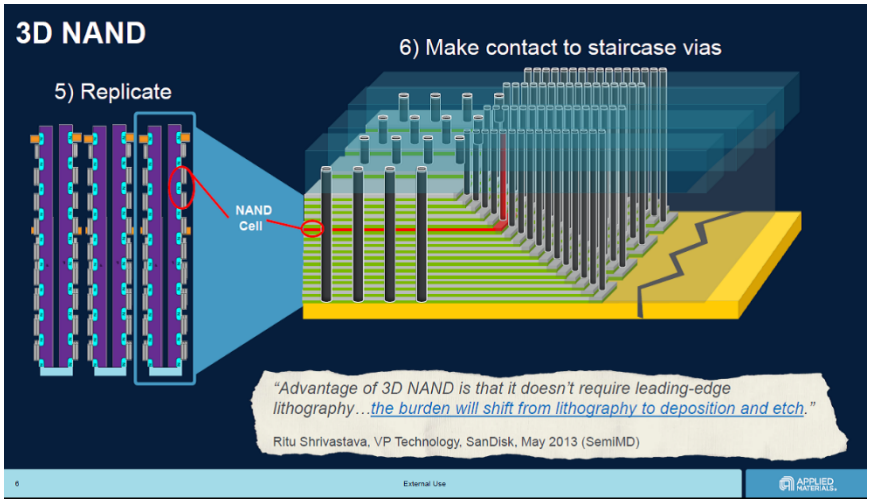
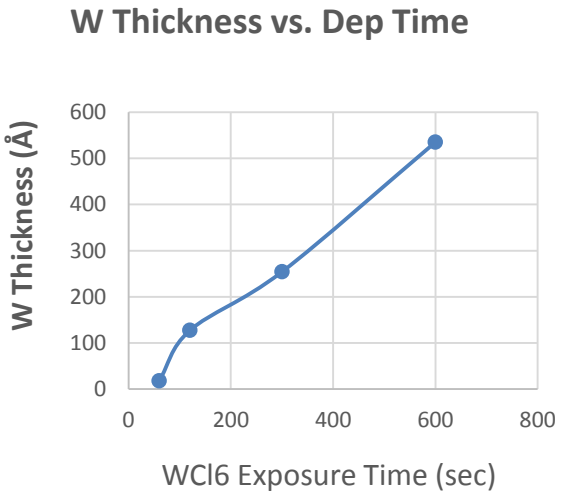
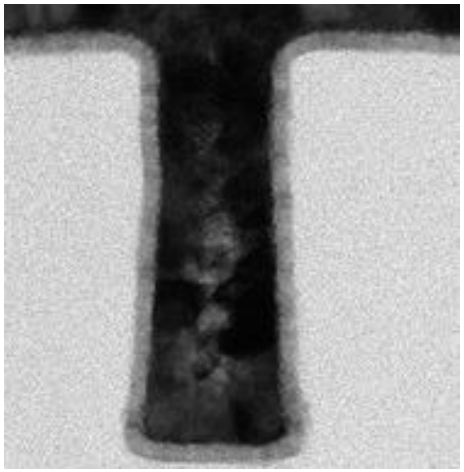
FFW (Fluorine Free W) for 3D NAND and Future Logic Nodes by CVD

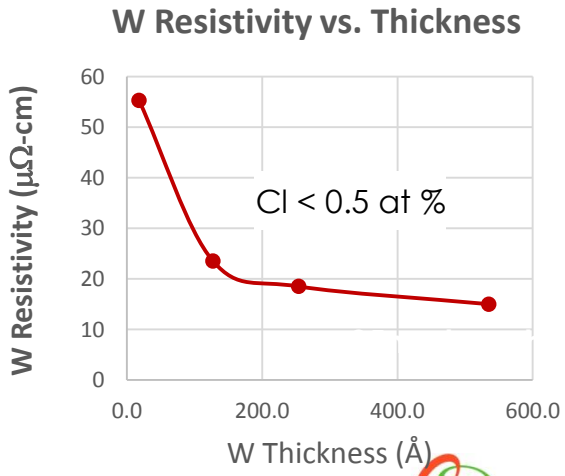


- WCl_6 purification is critical in achieving good film properties
- Solid delivery vessel enable delivering WCl_6
- Obtained CVD W above 400 °C. Higher temperature required to achieve low resistivity, low impurity level and faster deposition rate.





FFW Filled Via



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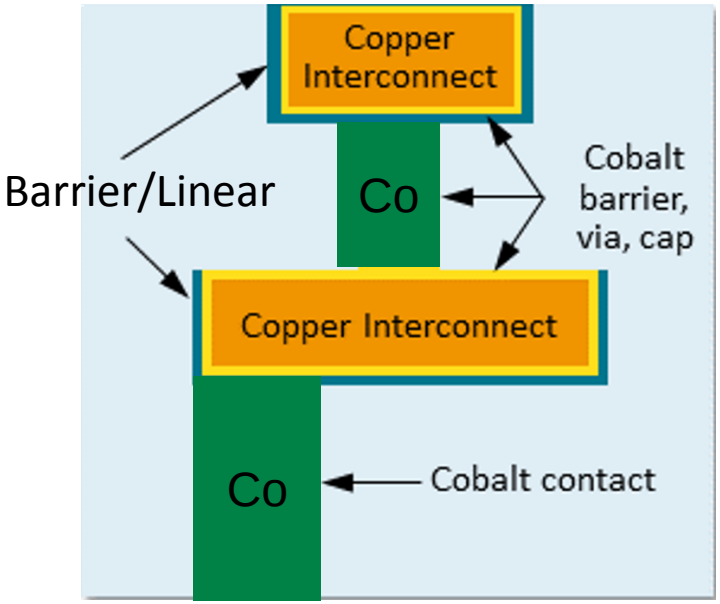
Selective Co CVD on Cu for Void-Free Via Fill Interconnect

Co Technology In advanced IC: BEOL today and beyond 10nm



CVD Co based Selective Growth for Void Free Via Fill

Ref. Jun-Fei Zheng et al, IITC 21015 (Entegris-Qualcomm-IMEC)

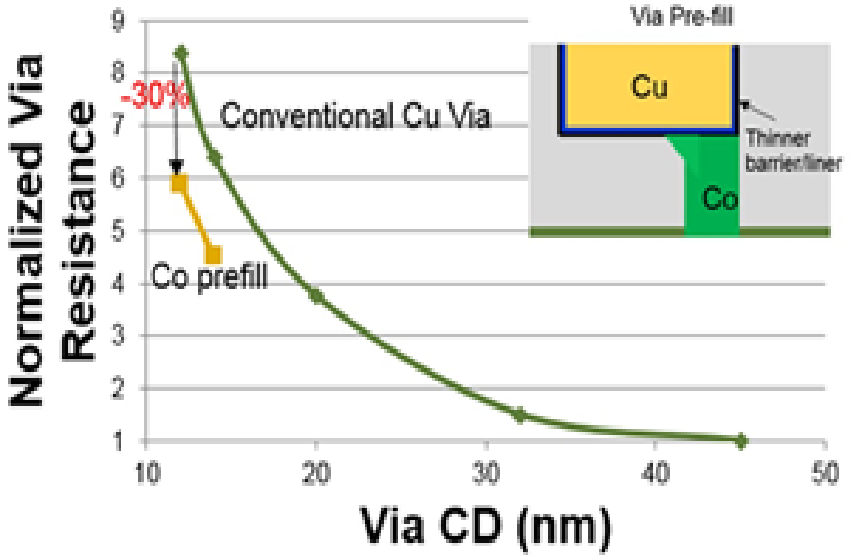


Fig. 1 Scaling of via resistance showing 30% via resistance reduction at 7nm BEOL

Co already being used successfully as barrier and cap. Now We are Exploring Co as via contact in 2X/1X high aspect ratio via in BEOL/MOL

Theoretical simulation shows that Co based via of 3:1 aspect ratio can reduce via resistivity by 30% as compared with Cu filled via with barrier/liner at via size of 10-15nm.

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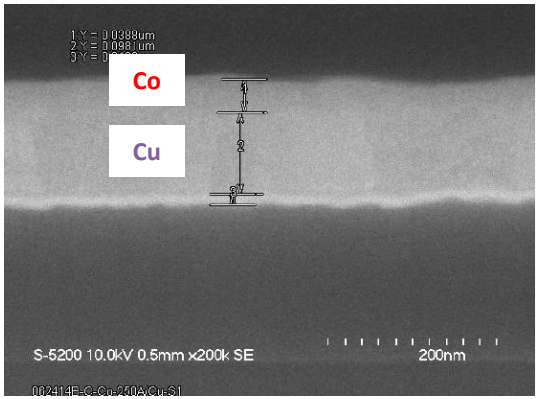
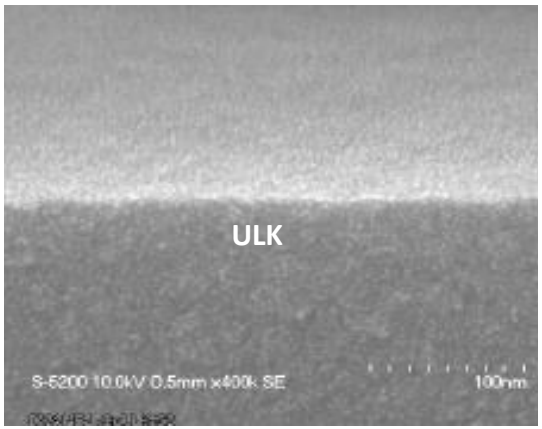
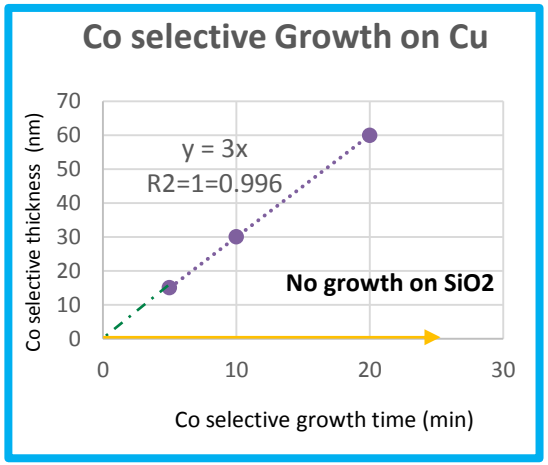
Selective CVD Co Deposition on Cu







Negligible Co on ULK

	C	N	O	F	Si	Co
ULK, 061414B-L, OACo; TOA = 25	24.7	0.2	48.1	0.6	26.3	0.1
ULK, 061414B-L, OACo; TOA = 45	24.0	0.1	49.1	0.6	26.1	0.1
ULK, 061414B-L, OACo; TOA = 75	23.9	0.2	48.8	0.7	26.2	0.2

Confirmed by angle-resolved XPS

Co growth is linear/

no incubation time,

No growth on ULK

Thickness measured by XRF

Selectivity Co on Cu / Co on ULK >> 300:1

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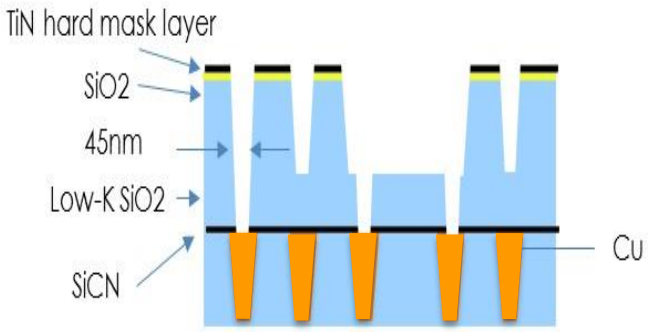
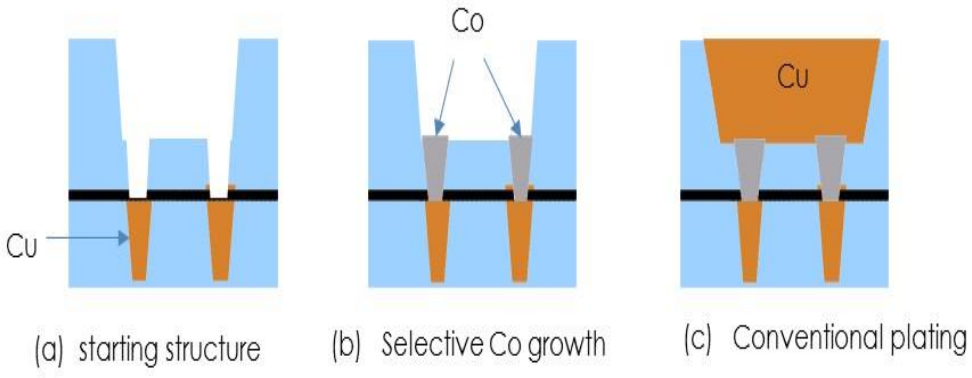
Process Integration

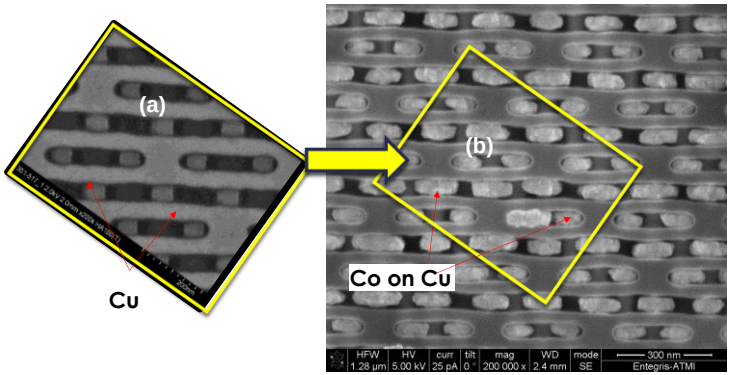
Selective CVD Co Growth on Cu
No Growth of Co on ULK

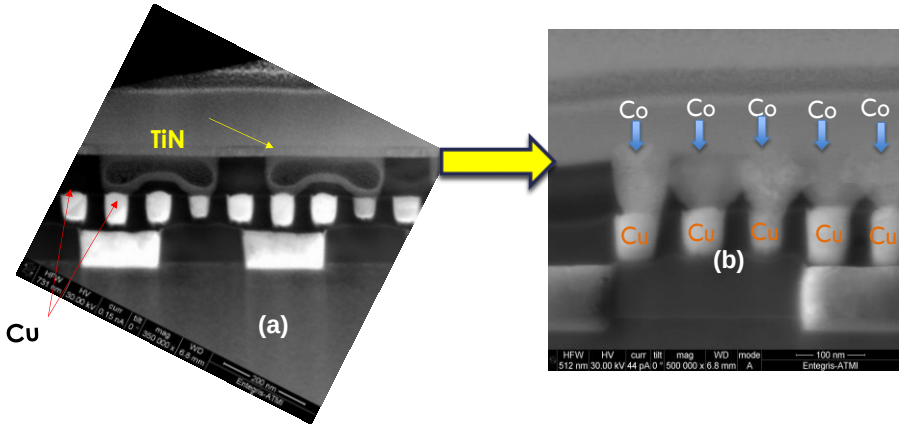




90nm pitch dual-damascene test structure. Via is 45nm 3:1 aspect ratio

Integration: (a)-> (b) Highly selective via fill by Co selective growth on Cu (c) Big trench structure can be filled by traditional Cu technology



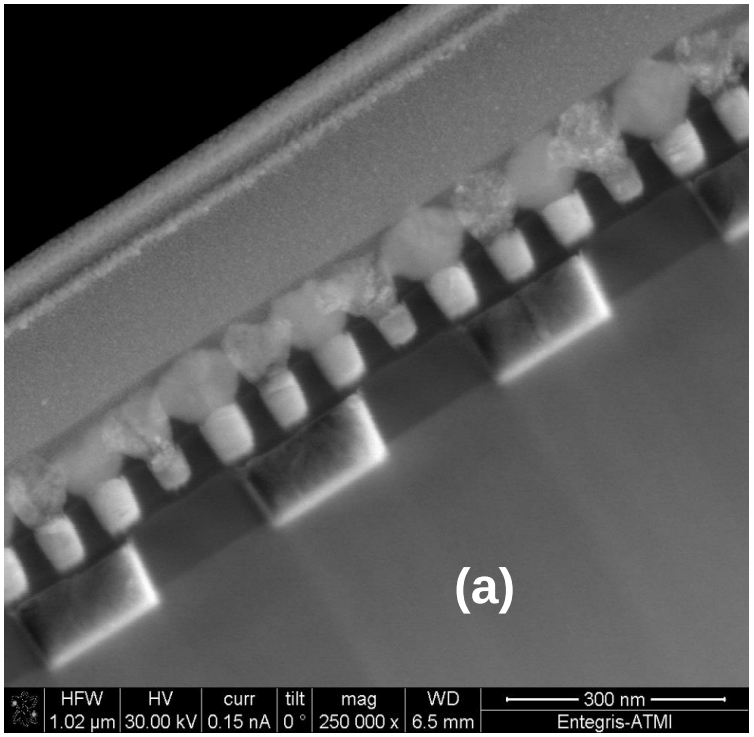


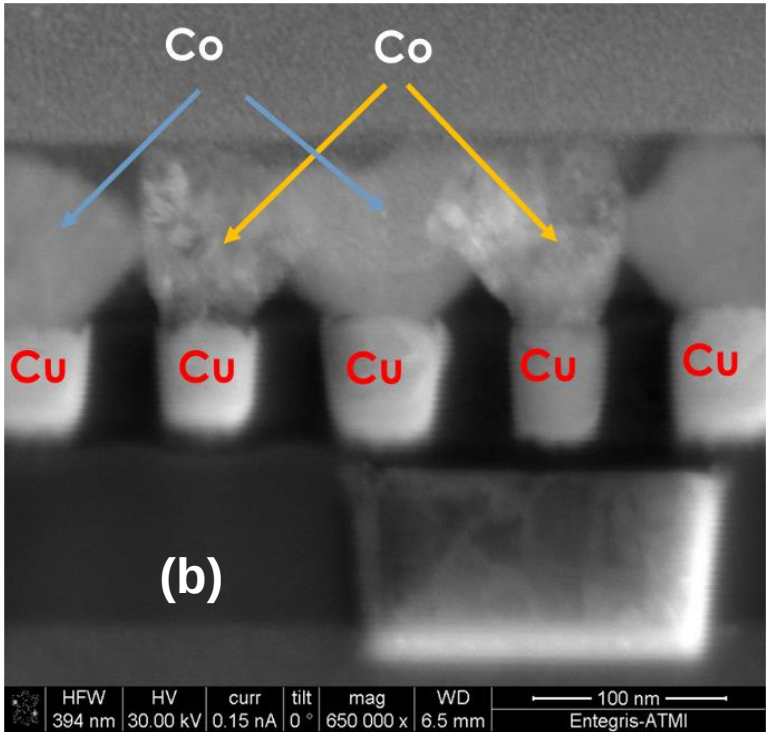
Top View: (a) As-received structure; (b) After Co selective deposition. Process temperature < 300 °C, easily compatible with frontend/M1 process.

Cross Section view; (a) before and (b) after Co selective deposition

Ref. Jun-Fei Zheng *et al,* IITC 21015 (Entegris-Qualcomm-IMEC)

No Voids/No Seam In Co Filled Via➔ Fine Grain Suggests Scalability Toward Smaller Bia of 2X/1X nm





(a) High resolution STEM image of the Co filled via. (b) Zoomed image of Co filled via. Note that the grain size is very fine <10nm

Ref. Jun-Fei Zheng *et al*, IITC 21015 (Entegris-Qualcomm-IMEC)

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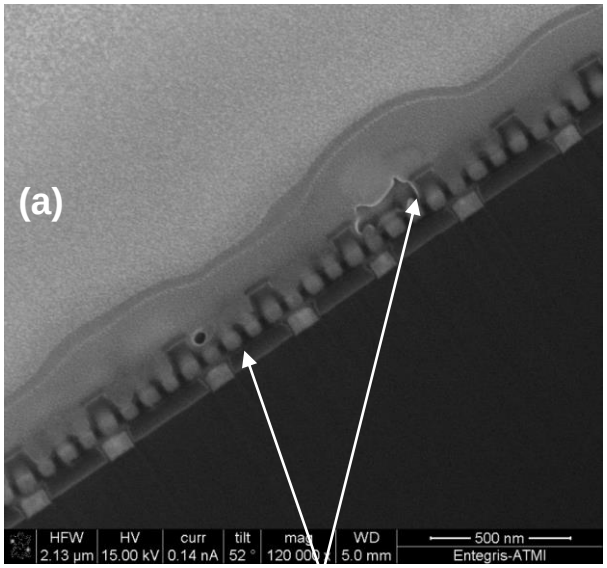
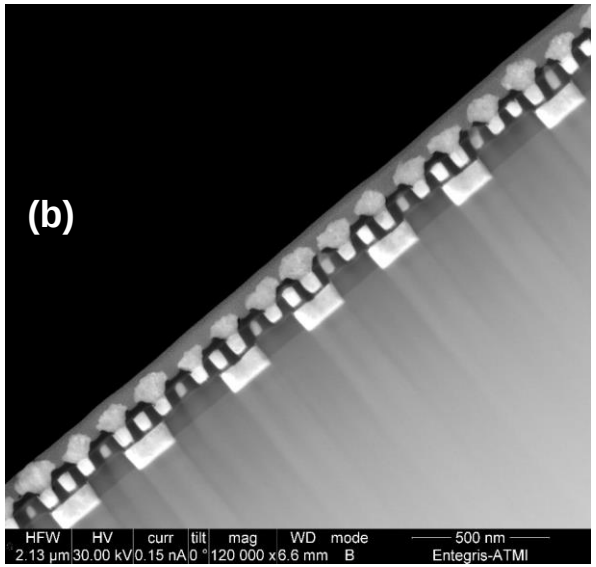
Wet Removal of TiN Prior To Selective CVD Co Deposition Is Critical

Without TiN wet clean



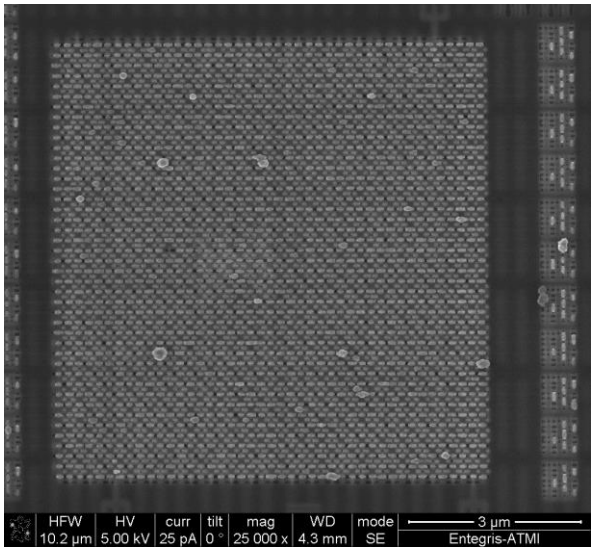
Random Defects

With TiN wet clean



No defects

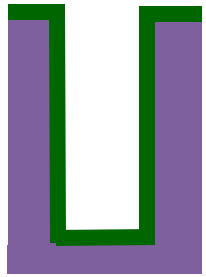
With TiN wet clean/Top View



Ref. Jun-Fei Zheng *et al,* IITC 21015 (Entegris-Qualcomm-IMEC)

Interconnect Metallization Using Electrolytic Cobalt Deposition

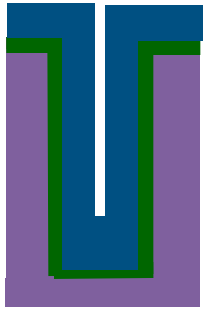
enthone®



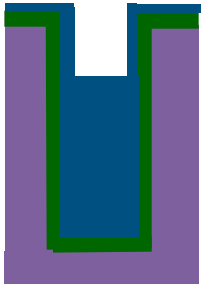
- A/R ≥ 8
- Opening ≤ 200 Å
- Co or Cu thin seed layer < 50 Å

Co VMS

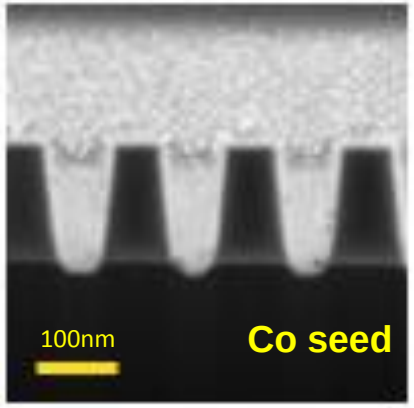
Co VMS + ENTHONE chemistry

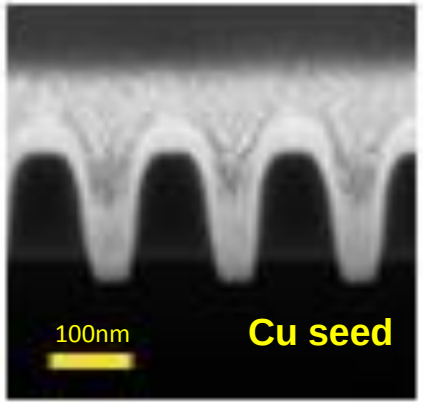


Conformal ✗



Bottom-Up ✓





enthone® chemistry provides:

- ❑ **Bottom-Up Fill : 2X/1X nm structures**
- ❑ **Low Resistivity: ≤ 15 µΩ·cm**
- ❑ **Low Stress**
- ❑ **High Purity: 2-10x VMS purity**

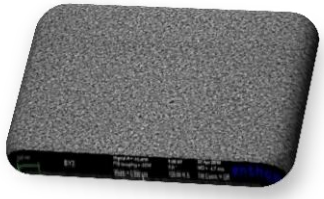
Entegris

Interconnect Metallization Using Electroless Cobalt Deposition

enthone®

Via pre-fill formulations with pH <9.5 (BEOL) Cu seed

400° C / 60 min	Sample 1	Sample 2
Time / thickness	150 sec / 38.8 nm	150 sec / 41.02 nm
Rs after Anneal	46.6 µΩ-cm	35.55µΩ-cm



Optimization ongoing for improved resistivity

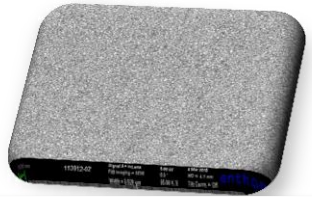
Non-selective & fill formulations with pH > 11.5 (MEOL) W seed

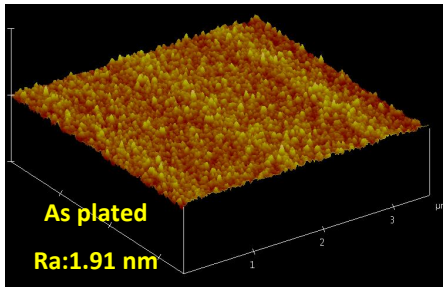
Parameter	Sample 1	Sample 2	Sample 3
Time / thickness	140 sec /46 nm	120 sec /37 nm	130 sec /48 nm
Rs as Plated	22.4 µΩ-cm	18.9 µΩ-cm	22.4 µΩ-cm
450C / 15 min	**15.9 µΩ-cm**	**13.6 µΩ-cm**	**17.0 µΩ-cm**

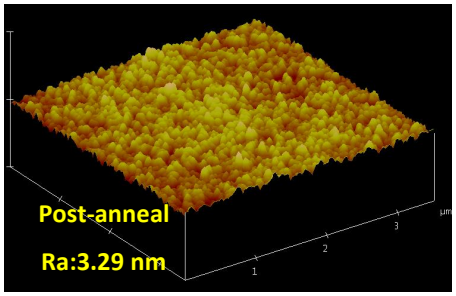
Excellent Resistivity

SIMS under ambient conditions

C	O	S	Cl	N	Other	Total impurity
279.69	2595.28	8.52	0.93	71.87	0.13	2956.42



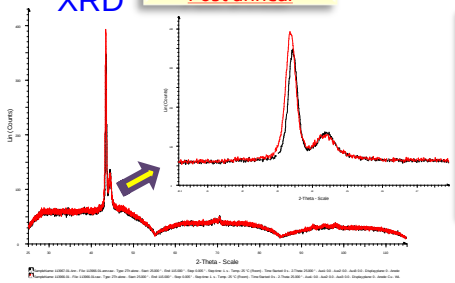




XRD

Before anneal

Post anneal



- Using beaker level scale we were able to demonstrate bottom-up via filling capability with candidate formulations mentioned above.

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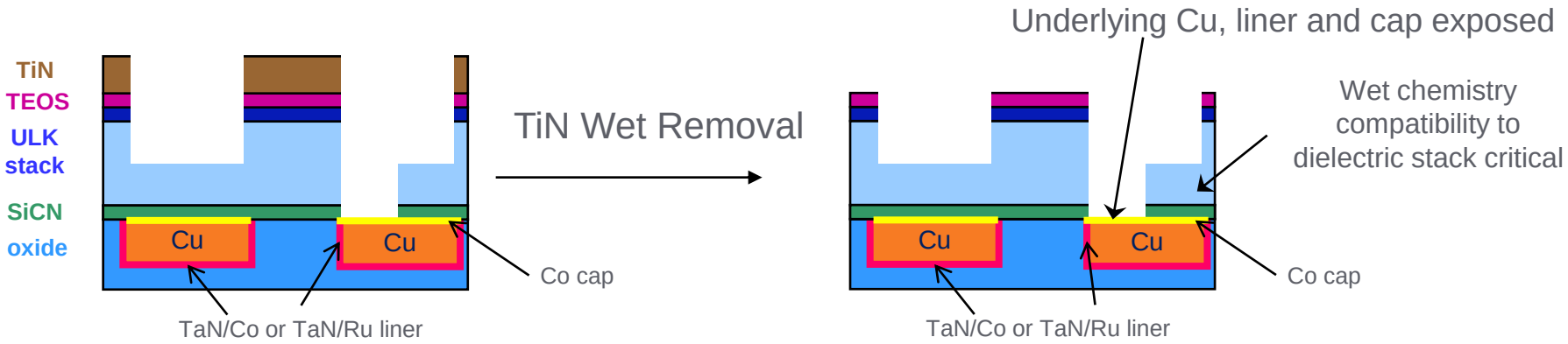
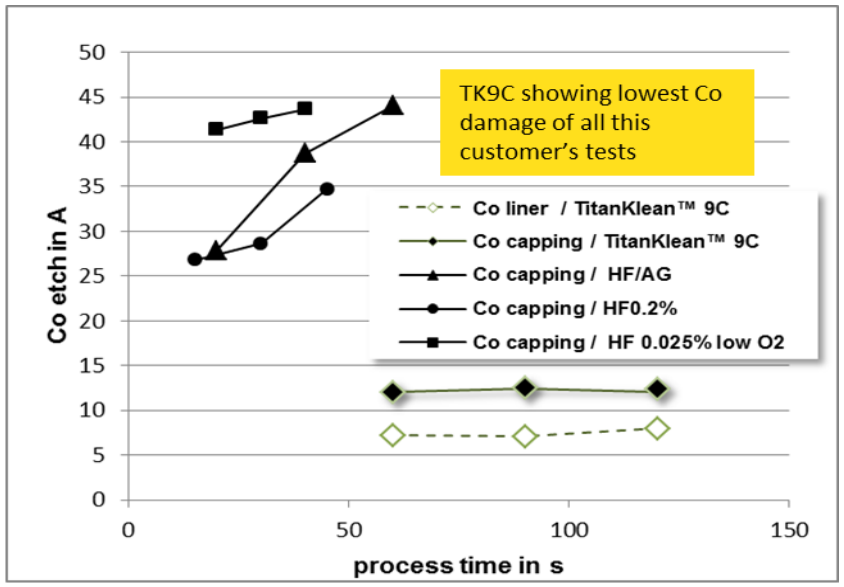
Entegris TiN Clean Solution Has Minimum Co Removal Rate In the BEOL Integration Process

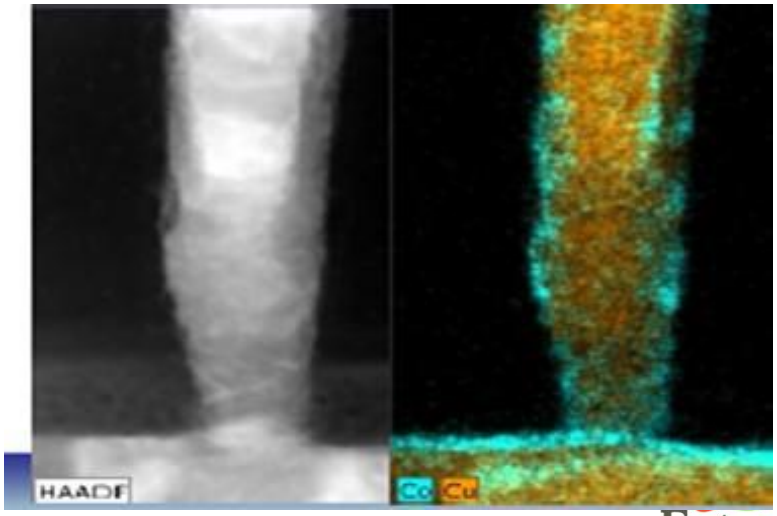


Post final etch

Co capping layer intact after cleaning and exposure to the TiN removal chemical



IITC 2015, "Cobalt compatible cleaning solutions for 14nm and beyond", Courabel et. al.



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Summary

- Advanced materials solutions are critically needed for beyond 10nm technology because of new materials and ever-evolving 3D device architectures

- Device, Equipment, and Material Companies should work together for the very challenge material solutions to reach device performance, yield, and cost targets

- As material solution provider, Entegris is working with device and equipment partners directly or via consortium in the frontier areas with the following examples for beyond 10nm solutions:
  - ✓ Ge surface passivation by wet chemicals, using electrical MOSCAP as an effective and efficient evaluation vehicle
  - ✓ Selective wet etch removal of GeSi in GeSi:Ge stack for the formation of Ge nanowires for gate-all-around FinFET at 5nm
  - ✓ As Conformal monolayer doping on Si and Ge surface achieve doping level that is meeting ITRS targets at 7/10nm
  - ✓ CVD Fluorine free W deposition for 3D NAND and future logic application
  - ✓ CVD Co selective growth on Cu for void free Via fill with expectation to work beyond 10nm technology
  - ✓ Advanced Electrolytic Co plating for replacing Cu in Cu dual-damasence interconnect
  - ✓ Electroless Co plating as an alternative approach for filling 2X/1X Via on Cu and W bottoms
  - ✓ Excellent TiN removal without impact to Co in the interconnect integration

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